CLAIMS

1.   A digital subscriber line transmission system using QAM modulation on several equally spaced discrete tones, wherein, at a high transmission rate, the system uses N = 2048/p or 4096/p tones spaced by 4.3125p KHz, where p is a power of 2.

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2.   The system of claim 1, wherein, for transmitting at a low transmission rate according to an ADSL standard, only the first n = 128 or 256 tones are used with p = 1.

3.   The system of claim 2, comprising, on the transmitter side:

10   an inverse fast Fourier transform (IFFT) circuit having N frequency domain value inputs corresponding to said tones, among which only the first receive values corresponding to the n used tones, the remaining inputs being zeroed,

        a decimator providing one sample for every r samples output by the IFFT circuit, with r = N/n, and

15   a digital-to-analog converter coupled between the decimator and a subscriber line.

4.   The system of claim 3, comprising, on the receiver side:

        an analog-to-digital converter sampling the signal on the subscriber line at a frequency F/r, where F is the operating frequency of the IFFT circuit;

20   an interpolator generating samples at frequency F from the samples provided by the analog-to-digital converter; and

        a fast Fourier transform (FFT) circuit operating at frequency F and receiving the samples from the interpolator through a time domain equalizer;

wherein, when all N tones are used, the time domain equalizer is bypassed.

5.   The system of claim 1, applicable to a standard using n first tones among the N tones, where n is a power of 2, comprising, at a transmitter side, an IFFT circuit having:

5   a number of frequency domain inputs selectable at least among values N and n; and

an operating frequency selectable at least among two values F and fn proportional, respectively, to the frequency of the last of the N tones at the high transmission rate, and to the last of the n tones.

10   6.   The system of claim 5, comprising, at a receiver side, an FFT circuit having:

a number of frequency domain outputs selectable at least among values N and n; and

an operating frequency selectable at least among values F and fn.

7.   The system of claim 6, wherein each of the IFFT and FFT circuits includes five

15   radix-4 stages and a last radix-2 or radix-4 stage connected to operate in pipeline mode, the desired number of frequency domain inputs or outputs of the circuit being selected by bypassing an appropriate number of stages and by selecting the radix of the last stage.